CLAIMS

What is claimed is:

1. A method, comprising:

detecting a data rate from an incoming data signal;

selecting an external reference clock frequency corresponding to the detected data rate;

frequency and phase locking to the incoming data stream;

and

automatically configuring a serializer to correspond to the detected data rate.

2. The method of Claim 1, wherein the automatically configuring a serializer to correspond to the detected data rate comprises:

initiating a time delay to configure the serializer from a LAN mode to a WAN mode.

3. The method of Claim 2, wherein in the time delay is 1.6 milliseconds.

4. The method of Claim 1, wherein the automatically configuring a serializer to correspond to the detected data rate comprises:

using a random algorithm to configure the serializer to a desired LAN or WAN mode.

5. An apparatus, comprising:

a data rate detection unit to sample a data rate from an incoming data signal;

a first frequency configuration unit operatively coupled with the data rate detection unit to receive a detected data rate from the data rate detection unit;

an oscillator to generate a plurality of reference clock frequencies;

a frequency selector unit coupled with the oscillator to select one of the reference clock frequencies;

a phase lock unit to phase lock the incoming data signal, the phase lock unit coupled with the first frequency configuration unit; and

a data rate select output coupled with the first frequency configuration unit to operatively link the first frequency configuration unit with a second frequency configuration unit of a remote device.

6. The apparatus of Claim 5, further comprising:

a timer to implement a time delay between a first time when the first frequency configuration unit detects a phase lock and a second time when the second frequency configuration unit of the remote device switches modes to correspond to the one of the reference clock frequencies that produced the phase lock.

7. The apparatus as set forth in Claim 6, wherein the time delay is approximately 1.6 milliseconds.

8. The apparatus as set forth in Claim 5, wherein the frequency that produces a phase lock is selected from the group consisting of approximately 10.31 GHz and approximately 9.95 GHz.

9. An apparatus, comprising:

a data rate selector input coupled with the frequency configuration unit to link the frequency configuration unit with a first frequency configuration unit of a remote device;

a second frequency configuration unit coupled with the data rate serial input; and

a frequency selector unit coupled with an external oscillator to select a reference clock frequencies produced by the oscillator.

10. The apparatus as set forth in Claim 9, wherein a frequency that phase locks an outgoing data signal is selected from the group consisting of approximately 10.31 GHz and approximately 9.95 GHz.

11. A system, comprising:

a bus,

a memory coupled with the bus,

a central processing unit coupled with the bus,

a serializer/deserializer chipset coupled with the bus, the chipset configured to receive and transmit data signals, wherein the serializer/deserializer chipset includes a serializer portion operatively coupled with a deserializer portion, the deserializer portion including:

a data rate detection unit to sample a data rate from an incoming data signal;

a first frequency configuration unit operatively coupled with the data rate detection unit to receive a detected data rate from the data rate detection unit; and

a first frequency selector unit coupled with an external oscillator to select a reference clock frequency generated by the oscillator.

12. The system of Claim 11, wherein the deserializer portion further includes:

a first phase lock unit to phase lock the incoming signal, the first phase lock unit coupled with the first frequency configuration unit to determine whether a phase lock has occurred; and

a data rate select output coupled with the first frequency configuration unit to operatively link the first frequency configuration unit with a second frequency configuration unit of a serializer portion of the serializer/deserializer chipset.

13. The system of Claim 12, wherein the serializer/deserializer chipset further includes:

a timer to implement a time delay between a first time when the first frequency configuration unit detects a phase lock and a second time when the second frequency configuration unit switches a frequency at which the serializer portion of the serializer/deserializer chipset transmits data to correspond to the one of the reference clock frequencies that produced the phase lock.

14. The system as set forth in Claim 13, wherein the time delay is approximately 1.6 milliseconds.

15. The system as set forth in Claim 12, wherein the frequency that phase locks the incoming signal is selected from the group consisting of approximately 10.31 GHz and approximately 9.95 GHz.

16. The system of Claim 12, wherein the serializer portion including the second frequency configuration unit further includes:

a data rate selector input coupled with the second frequency configuration unit to link the second frequency configuration unit with the first frequency configuration unit of the deserializer portion of the serializer/deserializer chipset; and

a second frequency selector unit coupled with the external oscillator to select a reference clock frequencies generated by the oscillator.

17. An apparatus, comprising:

means for generating a plurality of reference clock frequencies;

means for selecting one of the reference clock frequencies and attempting to phase lock an incoming signal sent from a remote device, the incoming signal containing at least data information;

means for determining whether a phase lock has occurred;

means for selecting another one of the reference clock frequencies and reattempting to phase lock the incoming signal if no phase lock occurred; and

means for automatically switching a frequency at which a serializer coupled with the data processing system transmits data to correspond to the one of the reference clock frequencies that produces a phase lock.

18. The apparatus as set forth in Claim 17, wherein the system further comprises:

means for implementing a time delay between a first time when a phase lock occurs and a second time when the frequency at which a serializer coupled with the data processing system transmits data is switched to correspond to the one of the reference clock frequencies that produced the phase lock.

19. The apparatus as set forth in Claim 18, wherein the time delay is approximately 1.6 milliseconds.

20. The apparatus as set forth in Claim 17, wherein the frequency that produces a phase lock is selected from the group consisting of approximately 10.31 GHz and approximately 9.95 GHz.

21. A computer readable medium containing executable computer program instructions, which when executed by a data processing system, cause the data processing system to perform a method comprising:

generating a plurality of reference clock frequencies;

selecting one of the reference clock frequencies,

attempting to phase lock an incoming data signal sent from a remote device:

determining whether a phase lock has occurred;

selecting another one of the reference clock frequencies and attempting a second time to phase lock the incoming signal if no phase lock occurred; and

automatically switching a frequency at which a serializer coupled with the data processing system transmits data to correspond to the one of the reference clock frequencies that produces a phase lock.

22. The computer readable medium as set forth in Claim 21, wherein the method further comprises:

implementing a time delay between a first time when a phase lock occurs and a second time when the frequency at which a serializer transmits data is

switched to correspond to the one of the reference clock frequencies that produced the phase lock.

23. The computer readable medium as set forth in Claim 22, wherein the time delay is approximately 1.6 milliseconds.

24. The computer readable medium, as set forth in Claim 21, wherein the frequency that produces a phase lock is selected from the group consisting of approximately 10.31 GHz and approximately 9.95 GHz.